

side by side

result set

DB=USPT; PLUR=YES; OP=ADJ

<u>L76</u>	pipeline adj stages and comparison adj logic and interface and memory	77	<u>L76</u>
<u>L75</u>	L71 and tag	3	<u>L75</u>
<u>L74</u>	L72 and tag	4	<u>L74</u>
<u>L73</u>	L72 and tagging	0	<u>L73</u>
<u>L72</u>	L68 and rate	5	<u>L72</u>
<u>L71</u>	L70 and rate	3	<u>L71</u>
<u>L70</u>	L67 and comparison adj logic	3	<u>L70</u>
<u>L69</u>	L68 and comparison adj logic	0	<u>L69</u>
<u>L68</u>	L67 and header	8	<u>L68</u>
<u>L67</u>	L66 and memory	38	<u>L67</u>
<u>L66</u>	pipeline adj interface and stages	44	<u>L66</u>
<u>L65</u>	pipeline adj stage adj interface	0	<u>L65</u>
<u>L64</u>	L63 and tagging	1	<u>L64</u>
<u>L63</u>	L61 and rate	10	<u>L63</u>
<u>L62</u>	L61 and tagging	1	<u>L62</u>
<u>L61</u>	L60 and flow	10	<u>L61</u>
<u>L60</u>	L59 and memory	10	<u>L60</u>
<u>L59</u>	L58 and header	10	<u>L59</u>
<u>L58</u>	pipeline adj stages and comparison adj logic and interfaces	77	<u>L58</u>
<u>L57</u>	L54 and input adj capacity	0	<u>L57</u>
<u>L56</u>	L54 and input adj rate	0	<u>L56</u>
<u>L55</u>	L54 and rate	1	<u>L55</u>
<u>L54</u>	pipeline adj stages and comparison adj logic and first adj interface and second adj interface	1	<u>L54</u>
<u>L53</u>	L52 and pipeline	0	<u>L53</u>
<u>L52</u>	comparison adj logic and interfaces and input adj capacity and size	1	<u>L52</u>
<u>L51</u>	L50 and tag and logic	58	<u>L51</u>
<u>L50</u>	L48 and flow	70	<u>L50</u>
<u>L49</u>	L48 and input adj flow	0	<u>L49</u>
<u>L48</u>	L44 and memory	72	<u>L48</u>
<u>L47</u>	L44 and comparison adj logic	0	<u>L47</u>
<u>L46</u>	L43 and size and input adj rate	0	<u>L46</u>
<u>L45</u>	L43 and size and input adj capacity	0	<u>L45</u>
<u>L44</u>	L43 and size and capacity	73	<u>L44</u>
<u>L43</u>	L42 and interface	216	<u>L43</u>
<u>L42</u>	pipeline adj stages and header	232	<u>L42</u>

<u>L41</u>	L40 and pipeline	0	<u>L41</u>
<u>L40</u>	input adj capacity and header and packet adj size	6	<u>L40</u>
<u>L39</u>	L37 and header	0	<u>L39</u>
<u>L38</u>	L37 and pipeline	0	<u>L38</u>
<u>L37</u>	input adj flow and memory and input adj capacity	4	<u>L37</u>
<u>L36</u>	L34 and capacity and size	22	<u>L36</u>
<u>L35</u>	L34 and input adj capacity	0	<u>L35</u>
<u>L34</u>	L30 and header	39	<u>L34</u>
<u>L33</u>	L32 and header	0	<u>L33</u>
<u>L32</u>	L30 and input adj rate	4	<u>L32</u>
<u>L31</u>	L30 and input adj capacity	0	<u>L31</u>
<u>L30</u>	L29 and interface	149	<u>L30</u>
<u>L29</u>	comparison adj logic and pipeline and stages	175	<u>L29</u>
<u>L28</u>	L26 and comparison adj logic	0	<u>L28</u>
<u>L27</u>	L26 and header	3	<u>L27</u>
<u>L26</u>	L25 and interface and packet adj size	4	<u>L26</u>
<u>L25</u>	L24 and stages	214	<u>L25</u>
<u>L24</u>	input adj rate and pipeline	287	<u>L24</u>
<u>L23</u>	input adj rate adj regulation and pipeline	0	<u>L23</u>
<u>L22</u>	L21 and header and interface	1	<u>L22</u>
<u>L21</u>	pipeline and stages and input adj capacity	16	<u>L21</u>
<u>L20</u>	L19 and header	0	<u>L20</u>
<u>L19</u>	L18 and input	14	<u>L19</u>
<u>L18</u>	L17 and comparison adj logic	14	<u>L18</u>
<u>L17</u>	L16 and capacity and size	561	<u>L17</u>
<u>L16</u>	pipeline adj stages and interface	1758	<u>L16</u>
<u>L15</u>	L14 and comparison adj logic	0	<u>L15</u>
<u>L14</u>	L13 and interface	8	<u>L14</u>
<u>L13</u>	input adj capacity and packet adj size	9	<u>L13</u>
<u>L12</u>	L11 and input adj capacity	0	<u>L12</u>
<u>L11</u>	pipeline adj stages and interface	1758	<u>L11</u>
<u>L10</u>	input adj capacity and interface and memory and header	13	<u>L10</u>
<u>L9</u>	input adj capacity and pipeline adj stages	0	<u>L9</u>
<u>L8</u>	L7 and capacity	5	<u>L8</u>
<u>L7</u>	L5 and packet adj size	33	<u>L7</u>
<u>L6</u>	L5 and input adj capacity	0	<u>L6</u>
<u>L5</u>	L4 and interface	1758	<u>L5</u>
<u>L4</u>	pipeline adj stages	2596	<u>L4</u>

<u>L3</u>	pipeline adj stages and interface and input adj capacity and packet adj size	0	<u>L3</u>
<u>L2</u>	pipeline and stages and interface	6036	<u>L2</u>
<u>L1</u>	compare and input adj capacity and packet adj size	2	<u>L1</u>

END OF SEARCH HISTORY